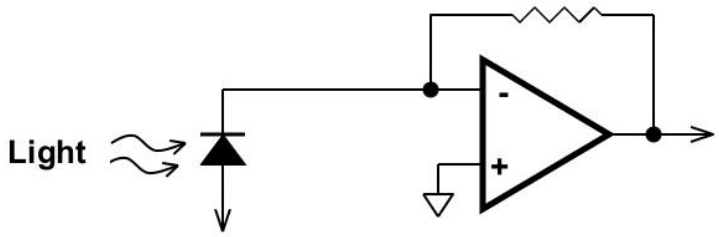
2018 PHY226 Electronics **Final Exam** **NAME: _____**

1. Optoelectronics: LEDs and photodiodes (20 points)

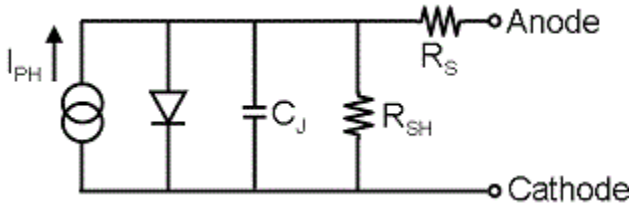
(A) LEDs and photodiodes are essentially just semi-conductor diodes which interact with electromagnetic waves. Explain their operation principle and why LEDs should be forward biased while photodiodes reversely biased?

(B) The simplest way to measure the light intensity is using a photodiode in the photoconductive mode:



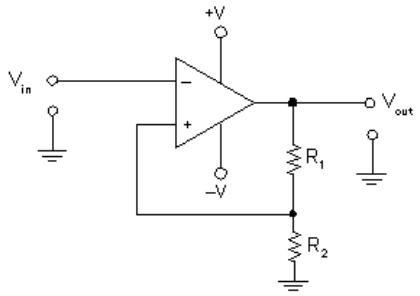
You are a solar physicist. Sun delivers about 1.0 kW/m^2 on the earth surface and you wish to study the solar activity by monitoring its intensity. You use the above circuit diagram with a photodiode (FDS010, Thorlabs, 0.8 mm^2 active area) and a resistor of 10 kΩ to measure the sun light. The output you get is about 1V, what is the quantum efficiency of the photodiode at the mean sunlight wavelength of 500 nm? (h=6.626×10^{-34} m^2 kg/s, e=1.60×10^{-19} C)

(C) It is predicted that the sun emits solar flares of various types that flash for 10 ps (flare pulse) to 1 ms (monster flare). In order to know whether your detector can see the flares, you look up FDS010 and found junction capacitance is CJ = 6pF, shunt resistance R_SH = 1 MOhm and series resistor = 500 Ohm. See effective diagram below. Estimate the range of the solar flash duration your photodector can record.



2. Converting an analog signal to a digital signal with a Schmitt trigger (20 points)

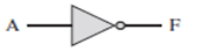
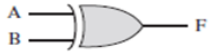
(A) The Schmitt trigger is designed to remove fluctuations near the analog to digital switching threshold. Assume the maximum output of the op-amp in the following circuit is +V = +5V and the minimum is –V = -5V, R1=15 kΩ, R2=10 kΩ, calculate the upper and lower switching threshold voltages.



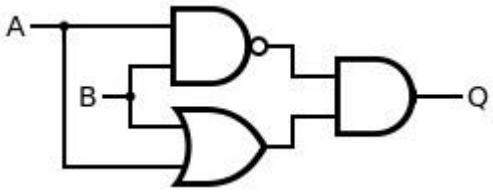
(B) Continue (A), if $V_{in}(t)$ = 5 Volt * sin ωt, draw the expected output waveform.

3. Digital gates and Boolean algebra (20 points)

Commonly used gates are summarized below

Name	Graphical Symbol	Algebraic Function	Truth Table
AND		$F = A \cdot B$ or $F = AB$	A B | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = A + B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
NOT		$F = \overline{A}$ or $F = A'$	A | F 0 | 1 1 | 0
NAND		$F = \overline{AB}$	A B | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR		$F = \overline{A + B}$	A B | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
XOR		$F = A \oplus B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0

(A) Complete the truth table of the following gate with possible inputs of A and B, and show that following circuit can be reduced to a single logic gate. What kind of gate is it?

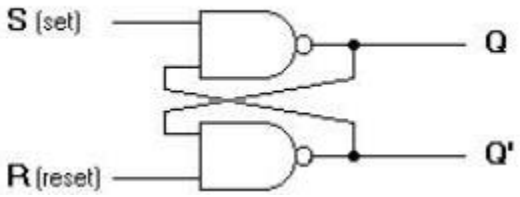


(B) Simplify the following Boolean expressions

- $\overline{\overline{A + B\overline{C}} + A\overline{B}}$
- $(A + 1)(A + \bar{A})$
- $\sum_{i=1}^{n} A^i$
- $A + AB + ABC + ABCD + ABCDE + \cdots$

4. Flip-flops (20 points)

Flip-flops are the fundamental memory units. At the center of them is the SR (set-reset) flip-flop, given in the diagram below in terms of two NAND gates. Such device can store 1 bit of information.



(A) Based on the truth table of the NAND gate (see question 3), show that the system develops a bistability Q=1 or 0 only when both S and R are 1.

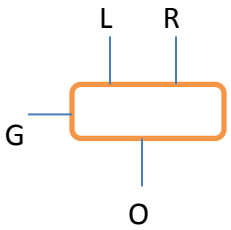
(B) Such bistability is the key of memory storage. If the information you wish to save is "0", describe the procedure you would use to set Q=0.

(C) In typical operation of SR flip-flop, the unused mode is S=R=0. What would be the outputs when S=R=0?

5. FPGA (Field Programmable Gate Array) (20 points)

Two key components in an FPGA are (1) construction of an arbitrary logic circuit and (2) rewiring. Here we will talk about the former.

A generic look-up table can be built based on repeated use of the following three terminal logic component, where L, R and G are digital inputs, and O is the output.



When the gate G = 1, output O connects to the left input L; when G=0 output O connects to right input R.

(A) Construct the truth table of such three-terminal logic gate for all possible inputs L, R, and G.

(B) Write down one Boolean expression that produces the truth table and construct the three-terminal gate based on fundamental gates shown in problem 3? (There are more than one solution, choose a simple one that reproduces the truth table.

(C) How would you build the generic look-up table using the 3-terminal gates described in (A)? Here A1, A2, A3 are inputs, O is output, and “a”, “b”….”h” are Boolean constants with of 0 or 1.

A1	A2	A3	O
0	0	0	a
0	0	1	b
0	1	0	c
0	1	1	d
1	0	0	e
1	0	1	f
1	1	0	g
1	1	1	h